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| 09/492,789 | 01/28/2000 | Takakazu Yano | 01165.0770 | 1372 |

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| EXAMINER | |
|---|---|
| JORGENSEN, LELAND R | |
| **ART UNIT** | **PAPER NUMBER** |
| 2675 | |

DATE MAILED: 04/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. 09/492,789 | Applicant(s) YANO ET AL. | |
|---|---|---|---|
| | Examiner Leland R. Jorgensen | Art Unit 2675 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *20 September 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1 - 6, 8 - 15, and 18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 - 6, 8 - 15, and 18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Objections*

1. In view of applicant's amendment, the objection to Claim 18 is withdrawn.

### *Claim Rejections - 35 USC § 112*

2. In view of applicant's amendment canceling Claim 7, the 35 U.S.C. 112, first paragraph, objection to Claim 7 is withdrawn.

### *Claim Rejections - 35 USC § 103*

3. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

4. Claims 1 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Beeteson et al., USPN 6,177,915 B1, in view of Nonomura et al., USPN 6,115,021.

#### Claim 1

Beeteson teaches a power supply circuit, which has a scan driver power circuit for supplying a scan driver voltage to a scan driver [row driver 7] for scanning a liquid crystal display device and which has a data driver power circuit for supplying a data driver voltage to a data driver [column driver 8] for sending display data to the liquid crystal display device [LCD panel 1]. Beeteson, col. 4, lines 15 – 26, and figure 4. Beeteson teaches a brightness control circuit [PROM 36], provided in the scan driver power circuit for controlling brightness of the liquid crystal display device by changing the voltage level of the scan driver voltage, specifically

by adding row correction value Y" to row brightness value Y'. Beeteson, col. 4, lines 26 – 44; and figure 4.

Although it is inherent that the data driver of Beeteson has a power circuit, Beeteson does not describe the details including the temperature compensation circuit.

Nonomura teaches a voltage regulation circuit for regulating the voltage level of the data driver voltage $V_d$ supplied to the liquid crystal display device to a predetermined value. Specifically, Nonomura teaches a voltage regulation circuit that includes a power supply section 36, reference voltage generation circuit 33, and buffer 34 to provide the data driver voltage $V_d$. The power supply section 36 generates a reference voltage $V_e$ to compensation reference voltage generation circuit 33. Voltage generation circuit 33 includes $R_1$ (fixed resister 31) in parallel with $R_0$ (resistance of temperature sensor 30), both in series with $R_2$ (fixed resister 32) to divide $V_e$. Buffer 34 amplifies the current. This circuit outputs data driver voltage $V_d$. Nonomura col. 11, lines 33 – 37; col. 12, lines 5 – 32; and figures 9 and 10. See also Nonomura, col. 12, line 49 – col. 14, line 4; and figures 11 – 13.

Nonomura teaches a temperature compensation circuit for compensating a temperature characteristic of the liquid crystal display device by changing the voltage level of the data driver voltage $V_d$. Specifically, Nonomura teaches that this temperature compensation circuit includes the temperature compensation power supply circuit 35 and the temperature sensor 30. Voltage generation circuit 33 includes $R_0$, (resistance of temperature sensor 30) in parallel with $R_1$ (fixed resister 31), both in series with $R_2$ (fixed resister 32) to divide $V_e$. Buffer 34 amplifies the current. This circuit outputs data driver voltage $V_d$. Nonomura col. 11, lines 33 – 37; col. 12,

lines 5 – 32; and figures 9 and 10. See also Nonomura, col. 12, line 49 – col. 14, line 4; and figures 11 – 13.

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the temperature compensation data driver power circuit as taught by Nonomura with the power supply circuit as taught by Beeteson to produce a large capacity display with a sufficiently high contrast that can be realized in a wider range of operation temperature. Nonomura invites such combination by teaching,

> In this example, the driving conditions for maintaining the memory angle at a constant angle can be obtained by provision of the temperature compensation power supply circuit 35. As a result, large capacity display with a sufficiently high contrast can be realized in a wider range of operation temperature.

Nonomura, col. 12, lines 33 – 38. See also: Nonomura, col. 6, lines 38 – 45; and col. 13, line 65 – col. 14, line 4.

**Claim 18**

It is inherent that the data driver power circuit [temperature compensation power supply circuit 35] shown by Nonomura in figures 9 and 10 would perform voltage regulation, temperature compensation, and power supply functions at the same time. Nonomura, col. 12, lines 5 – 32; and figures 9 and 10.

5. Claims 2, 8, and 13 - 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Beeteson et al. in view of Nonomura et al. as applied to claim 1 above, and further in view of Nishioka et al., USPN 6,121,943.

**Claim 2**

Nonomura teaches an input power supply [power supply section 30] serving as a universal power supply. Nonomura, col. 12, lines 15 – 18; and figure 9. An amplifying element [buffer circuit 34 formed of an operational amplifier] has an input terminal connected to the input power supply and a control terminal and an output terminal from which the data driver power voltage $V_d$ is outputted. Nonomura, col. 12, lines 19 – 32; and figure 10. An impedance element [fixed resistor 31] is connected between the input power circuit and the control terminal of the amplifying element. The voltage regulation circuit [compensation reference voltage generation circuit 33] and the temperature compensation circuit [temperature sensor 30] is connected to the control terminal of the amplifying element. Nonomura, col. 12, lines 5 – 32; and figures 9 and 10.

Neither Beeteson nor Nonomura teach the divider circuit between the input power supply and the ground for setting a voltage applied to the control terminal of the amplifying element.

Nishioka teaches a divider circuit between the input power supply and the ground for setting a voltage applied to the control terminal of the amplifying element. Nishioka, figures 4 and 6, col. 5, line 59 - col. 6, line 5. Nishioka teaches a variable resister 81b having a resistance variation terminal connected to the control terminal of the amplifying element. Nishioka, figures 4 and 6, col. 5, line 59 - col. 6, line 5.

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the constant current control circuit of Nishioka to the display voltage supply circuit of Beeteson and Nonomura to create a scan driver power circuit. Nishioka points out that "It is an object of the present invention to solve the problems associated with the generation of heat

and the rush current during the application of the scan signal while reducing the charging and discharging time." Nishioka, col. 1, lines 54 – 57. Nishioka teaches the advantage of its power circuit for scan driver. "Thus, the constant current control circuit 81 performs control to provide a constant current in response to the control signal at a high level input from the input terminal S1. Nishioka, col. 6, lines 2 – 5.

**Claim 8**

Nishoika teaches a resister 81c having a terminal connected to the input power supply. Nishioka, figures 4 and 6, col. 5, line 59 - col. 6, line 5. Nishioka teaches a Zener diode 81d having a cathode connected to the resister and an anode to ground. Nishioka, figures 4 and 6 and col. 6, lines 19 – 21.

**Claim 13**

Nonomura teaches that the amplifying element is an operational amplifier. Nonomura, col. 12, lines 21 – 26.

**Claim 14**

Nishioka teaches the use of bipolar transistors in the scan driver and the data driver. Nishioka, col. 8, lines 44 – 48.

**Claim 15**

Nishioka teaches the use of field effect transistors (FET). Nishioka, col. 5, line 59 – col. 6, line 5.

6. Claims 3 – 6 and 9 – 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Beeteson et al. in view of Nonomura et al. and Nishioka et al. as applied to claim 2 above, and further in view of Sakamoto et al., USPN 3,956,661.

**Claim 3**

Neither Beeteson, Nonomura, nor Nishioka teach that the voltage regulation circuit and the temperature compensation circuit comprise a diode group.

Sakamoto teaches a voltage regulation circuit and the temperature compensation circuit that comprise a diode group having a plurality of series connected diodes connected between the control terminal of an amplifying element and ground. Sakamoto, figure 1; col. 2, lines 22 – 33. Sakamoto teaches a voltage regulation circuit and temperature compensation circuit. Sakamoto, figure 1; col. 2, lines 22 – 33. The temperature compensation circuit is connected to the control terminal of an amplifying element, a transistor 1 with a collector, base, and emitter. Sakamoto, figure 2; col. 2, lines 22 – 33.

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the voltage regulation and temperature compensation circuit as taught by Sakamoto with the data drive power circuit as taught by Beeteson and Nonomura to create a temperature compensation data drive power circuit having a stable output voltage in varying temperature. Sakamoto invite such combination by teaching,

> The present invention relates to an improved D.C. power source for stabilizing an output voltage and/or current especially in integrated circuits (IC) and also for compensating for deviation or fluctuation in the current amplification factor $h_{FE}$ or $\beta$ of a transistor due to variation in the ambient temperature.
>
> Heretofore, in a transistor circuit for supplying constant output voltage, a power supply voltage was divided by a pair of bias resistors including an emitter resistor in a transistor circuit built in an integrated circuit block, and the divided

> voltage was supplied to a transistor or transistors also built in the integrated circuit blocks. However, in a prior D.C. power source the compensation for preventing the change of the output voltage due to temperature change was not enough because the values of the resistances in the IC blocks were considerably varied by discrepancies among resistors as well as temperature variations, and it was very difficult to construct a transistor circuit in which an absolute value of the current flowing through a load was maintained constant.

Sakamoto et al., col. 1, lines 5 – 10. Sakamoto adds,

> A main purpose of the present invention is, therefore, to provide a D.C. power source having a temperature compensation circuit in which variation in the voltage drop between the base and emitter of a transistor due to variation in the ambient temperature is compensated.
>
> Another purpose of the present invention is to provide a D.C. power source having a temperature compensation circuit in which variation or deviation of the current amplification factor $h_{FE}$ or β due to variation in the ambient temperature is compensated.
>
> A still further purpose of the present invention is to provide a D.C. power source having a temperature compensation circuit in which the effect of variation in the ambient temperature on the output voltage and/or current compensated.

Sakamoto, col. 1, lines 29 – 45.

**Claim 4**

Sakamoto teaches that the series-connected diodes with a first diode having a cathode terminal connected to the control terminal of the amplifying element and a second diode with an anode terminal connected to the ground respectively. Sakamoto, figure 1; col. 2, lines 22 – 33.

**Claim 5**

Sakamoto teaches a circuit where the sum of the voltage drop of each diode, the voltage $V_{B1}$ at the junction point (a), is equal to the data driver voltage $V_{E1}$. Sakamoto, col. 4, lines 2 – 6.

**Claim 6**

It would have been obvious to one of ordinary skill in the art at the time of the invention to use seven diodes in the diode group. Sakamoto invites one to vary the number of diode. After defining *m* as the number of diode between the control terminal and ground, Sakamoto states,

> As described above, whenever the dividing ration of the D.C. power supply voltage $V_{CC}$ is desired, the first and second resisters R1 and R2 and values of *m* and *n* are in turn determined. Thus the effect of the change of the voltage drop between the base and emitter $V_{BE}$ of the transistor 1 due to temperature change is completely avoided by inserting a predetermined number of diodes 6.

Sakamoto, col. 3, lines 17 – 24. For one of ordinary skill in the art at the time of the invention, it is an obvious design choice, as motivated by the above teachings of Sakamoto, to choose a certain number of diodes to set an appropriate voltage drop.

**Claim 9**

Sakamoto teaches that the amplifying elements are transistors. Sakamoto, figure 2, col. 2, lines 22 – 33. Although Sakamoto does not specifically state in the specifications that the transistors are bipolar, bipolar transistors would be inherent because the symbol of the transistor used in Sakamoto's figures are those typically used for bipolar transistors.

**Claim 10**

It would have been obvious to one of ordinary skill in the art at the time of the invention to use such a range. Sakamoto invites one to consider different resistances. Sakamoto, col. 3, lines 17 – 24. Sakamoto offers formulas to find such resistances. Sakamoto, col. 2, line 21 – col. 3, line 32. For one of ordinary skill in the art at the time of the invention, it is an obvious design choice, as motivated by the above teachings of Sakamoto, to choose a certain resistance to produce an appropriate current.

**Claim 11**

It would have been obvious to one of ordinary skill in the art at the time of the invention to use silicon diodes for the diodes of the diode group. Silicon diodes are readily available and well know in the art, as admitted in applicant's specification, page 2, lines 11 – 12.

7. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Beeteson et al. in view of Nonomura et al. and Nishioka et al. as applied to claim 2 above, and further in view of The Electrical Engineering Handbook.

**Claim 12**

Neither Beeteson, Nonomura, nor Nishioka teaches that the amplifying elements are MOS transistors.

The Electrical Engineering Handbook teaches the use of MOS transistors. Handbook, p. 567 – 580.

It would have been obvious to one of ordinary skill in the art at the time of the invention to use MOS transistors for transistors in the data driver power circuit of Beeteson and Nonomura. The Handbook teaches that MOS transistors allow easy fabrication using lithographic processes, resulting in integrated circuits (ICs), with very small devices, very large device counts, and very high reliability at low cost. MOS transistors also allow manufacture of complex systems without expensive packaging or cooling requirements. Handbook, p. 568.

***Response to Arguments***

8. Applicant's arguments filed 20 September 2004 have been fully considered but they are not persuasive.

Applicants argue that Nonomura does not teach either a "voltage regulation circuit" or "temperature control circuit." Specifically, applicants argue that the temperature sensor output is sent to the temperature compensation power supply circuit 35 rather than changing the voltage level of the said data driver voltage. Applicants also argue that the compensation reference voltage generation circuit 33 supplies voltage to buffer 34 rather than "regulating the voltage level of said data driver voltage." This argument is unpersuasive. Ultimately, both circuits are designed to change and regulate the voltage level of the data driver voltage $V_d$. The discussion of Nonomura in claim 1 above has been clarified to show that both circuits directly change and regulate the voltage level of the data drive voltage.

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leland R. Jorgensen whose telephone number is 571-272-7768. The examiner can normally be reached on Monday through Friday, 10:00 am through 6:00 pm..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sumati Lefkowitz can be reached on 571-272-3638. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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DENNIS-DOON CHOW
PRIMARY EXAMINER